PowerPC 403GA, 403GB and 403GC Embedded Controllers

**Highlights**

**Bus Interface**
- Direct-connect peripheral/ROM and DRAM interfaces
- Support for 8-, 16- and 32-bit devices
- Addressing for main memory storage:
  - 192MB (403GB)
  - 512MB (403GA and 403GC)
- External bus master support using the internal DRAM controller
- IEEE 1149.1 (JTAG) compatible interface, for test, debug and real-time trace support

**DMA Controller**
- Independent DMA channels:
  - Four (4) (403GA and 403GC)
  - Two (2) (403GB)
- Buffered, fly-by, memory-to-memory modes
- Programmable for 8-, 16- and 32-bit transfers
- Data chaining

**Interrupt Controller**
- Low latency interrupt handling (three cycles typical)
- Six external interrupt inputs (five regular, one critical)
- Dual level interrupt structure for robust debug

**Instruction Fetch, Branch and Dispatch Unit**
- Four instruction prefetch queue
- Branch folding and static branch prediction
- Dispatches up to two instructions per cycle

**Serial Port (403GA & 403GC only)**
- RS-232 serial communications
- Programmable to 1.5 Mb/s

**Memory Protection**
- Device protection
- Address protection

**Instruction and Data Caches**
- Separate 2KB instruction and 1KB data caches
- Two-way set-associative
- Fetch-thru instruction cache
- Write-back data cache

**Timers**
- 56-bit time base (403GA and 403GB)
- 64-bit time base (403GC)
- 32-bit programmable interval timer
- Fixed interval timer
- Watchdog timer for system error recovery

**Power Management Capability**
- Static low-power design
- Dynamic power management and stand-by mode
- Support 3.3V and 5V peripherals

**Memory Management Unit (403GC only)**
- Memory Management Unit is precache (cache tags are physical addresses)
- 8 page sizes (1K-16M by powers of 4) for efficient system memory use
- 64 entry fully associative TLB with software replacement
- 16 protection zones
- Efficiently designed to minimize die area

**Product Description**

PowerPC 403GA*, 403GB* and 403GC* 32-bit RISC Embedded Controllers combine high performance and functional integration with low power consumption. On-chip caches and integrated device control functions reduce system chip count and design complexity, while improving system throughput.

These embedded controllers execute programs at sustained speeds approaching one instruction per cycle. Their RISC processor cores are tightly coupled to internal 2KB instruction and 1KB data caches, reducing overhead for data transfers to and from main storage. Instruction queue logic minimizes pipeline stalls by managing branch prediction, branch folding and instruction prefetching.

The PowerPC 403GC includes an integrated MMU featuring a fully associative TLB. Each entry provides translation for a memory page, which can be one of several sizes. TLB replacement is managed by software, which can employ the optimum replacement strategy for a particular application.

All 403 Embedded Controllers implement the PowerPC Architecture* in IBM’s 0.5 µm CMOS technology. These embedded controllers provide low-power 3.3V operation, with built-in stand-by mode and dynamic power management.
### PowerPC 403GA, 403GB and 403GC Specifications

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>0.5 µm CMOS, 3 levels of metal</td>
</tr>
<tr>
<td><strong>Number of Transistors</strong></td>
<td>~ 585,000 (403GA), ~ 500,000 (403GB), ~ 635,000 (403GC)</td>
</tr>
<tr>
<td><strong>Max Case Temp. Range</strong></td>
<td>0°C to 85°C</td>
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<tr>
<td><strong>Signal I/Os</strong></td>
<td>126 (403GA and 403GC)</td>
</tr>
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<td></td>
<td>104 (403GB)</td>
</tr>
<tr>
<td><strong>Power Supply</strong></td>
<td>3.3V ±5% (support for 5V I/Os)</td>
</tr>
<tr>
<td><strong>Performance</strong></td>
<td>56 MIPS (Dhrystone 2.1) @ 40MHz (403GA and 403GC)</td>
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<tr>
<td></td>
<td>39 MIPS (Dhrystone 2.1) @ 28MHz (403GB)</td>
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<tr>
<td><strong>Performance/Power</strong></td>
<td>175 MIPS/W (Dhrystone 2.1) (403GA and 403GC)</td>
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<td></td>
<td>186 MIPS/W (Dhrystone 2.1) (403GB)</td>
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<tr>
<td><strong>Power Dissipation (typ.)</strong></td>
<td>320 mW @ 40MHz (403GA and 403GC)</td>
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<tr>
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<td>210 mW @ 28MHz (403GB)</td>
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<tr>
<td><strong>Packaging</strong></td>
<td>160-pin plastic quad flat pack (403GA and 403GC)</td>
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<tr>
<td></td>
<td>128-pin thin quad flat pack (403GB)</td>
</tr>
<tr>
<td><strong>Frequency</strong></td>
<td>25, 33 or 40MHz (403GA and 403GC)</td>
</tr>
<tr>
<td></td>
<td>28 MHz (403GB)</td>
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</tbody>
</table>

The PowerPC 403GA, 403GB and 403GC are supported by IBM and over 75 select third-party vendors in the PowerPC Embedded Tools* program. This program offers a full range of embedded development tools, including compilers, debuggers, real-time operating systems, emulators, logic analyzers, and evaluation boards.

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**Diagram:**

```
  Int. Ctrl.  | JTAG Port  | Trace Port (403GA & 403GC) | Serial Port (403GA & 403GC) | DMA Controller (4-CH (403GA & 403GC) & 2-CH (403GB)) |
  |            |            |                         |                             |
  +------------+------------+---------------------------+-----------------------------+---------------------------------------------------|
  |            |            | RISC Execution Unit       | Memory Management Unit (403GC only) | Instruction Cache Unit | Data Cache Unit |
  |            |            | Timers                    |                             |                      |
  +------------+------------+---------------------------+-----------------------------+---------------------------------------------------|
  |            |            | Bus Interface Unit        | DRAM Controller             | I/O Controller       |
  |            |            |                           | Data Bus                   | Address Bus          |
```

**Notes:**

* Indicates a trademark or registered trademark of the International Business Machines Corporation.

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